

DIMM-Argon

Hardware Manual

Review V1



All rights reserved. This documentation may not be photocopied or recorded on any electronic media without written approval. The information contained in this documentation is subject to change without prior notice. We assume no liability for erroneous information or its consequences. Trademarks used from other companies refer exclusively to the products of those companies.

Revision: **Nr. / Datum**

Rev.	Date/Signature	Changes
1	2024-04-04/Bue	Initial Release
2		
3		

Content

1	Overview	4
1.1	Introduction.....	4
1.2	Block Diagram	4
2	Handling Precautions	5
3	Functions.....	6
3.1	Processor	6
3.1.1	General Information.....	6
3.1.2	Boot Mode.....	6
3.1.3	JTAG.....	6
3.1.4	RAM, Flash	6
3.1.5	Power Supply.....	7
3.1.6	Display	7
3.1.7	Touch Interface	8
3.1.8	Camera, VIO0.....	9
3.1.9	Audio.....	10
3.1.10	Ethernet.....	10
3.1.11	USB Host, Device	10
3.1.12	UARTs.....	12
3.1.13	CAN.....	12
3.1.14	SDC Interface	13
3.1.15	SPI.....	13
3.1.16	I2C	13
3.1.17	RTC.....	14
3.1.18	Status LEDs	14
3.1.19	Analog Inputs.....	14
3.1.20	Digital GPIOs	15
3.1.21	Reset.....	15
4	Connectors	Fehler! Textmarke nicht definiert.
4.1	P1, SODIMM Connection	16
4.2	J2, SODIMM Extension2.....	19
4.2.1	JP1, JTAG Connector	20

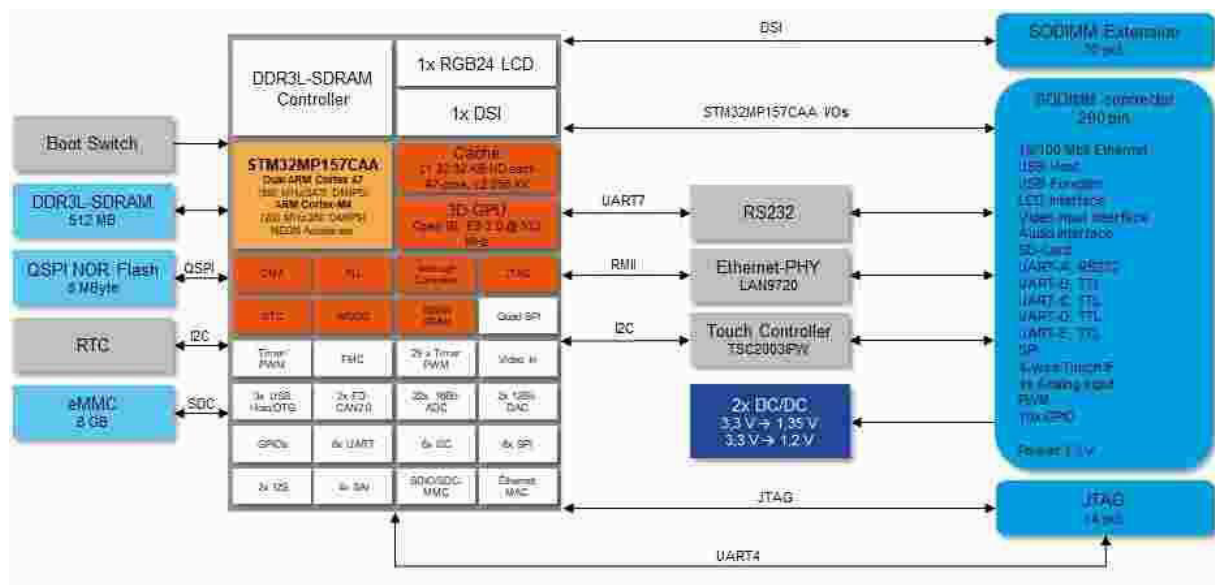
5	Technical Properties	20
5.1	Energy Supply	20
5.2	Ambient Conditions	20
5.3	Mechanical Specifications	20
6	Dimensional Drawing	21

1 Overview

1.1 Introduction

The DIMM-Argon module is a CPU module suitable for the emtrion DIMM family based on the STM32MP157CAA3 or STM32MP157FAA1 processor from ST Microelectronics. In principle, both processors can be fitted alternatively.

1.2 Block Diagram



The properties of the module are described in more detail below.

2 Handling Precautions

Please read the following instructions before installing the CPU module on your base board. They apply to all ESD (electrostatic discharge) sensitive components:

- Before touching the motherboard, you should discharge yourself by touching an earthed object.
- Make sure that all tools required for the installation are also electrostatically discharged.
- Disconnect the mains cable from the main power supply before installing (or removing) a CPU module.
- Also switch off the power supply before connecting or disconnecting cables to non-ESD-protected connections.
- Handle the circuit board with care and avoid touching its components or conductor tracks.

3 Functions

3.1 Processor

3.1.1 General Information

In principle, the two components STM32MP 157CAA3 and STM32MP 157FAA1 meet the requirements. They differ in maximum clock frequency and temperature range.

The C processor has 650 MHz and -40 to +125°C. For the F processor it is 800 MHz and -20 to +105°C. The component has a BGA448 design with a pitch of 0.8 mm.

Both processors can be fitted with alternative customer-specific components.

3.1.2 Boot Mode

The processor can boot from various flash memories (eMMC, SD card, NOR flash) and via the USB device interface. The boot device is selected using the 3-way DIP switch SW1.

This allows 8 combinations to be set, 5 of which are valid:

SW1-3	SW1-2	SW1-1	Boot Device
On	On	On	USB Serial Download
On	On	Off	QSPI NOR Flash Boot
On	Off	On	eMMC Boot
Off	On	On	Engineering Boot
Off	On	Off	SD Card Boot

The SD card is booted via the SODIMM SDC1 interface.

3.1.3 JTAG

For development purposes, the JTAG interface of the processor is connected to a 14-pin connector on the board.

The connector corresponds to the STDC14 specification from ST Microelectronics, see chapter 5.2.1.

In addition to the JTAG signals, UART4 is also routed to the connector. STLINK-V3 debuggers support JTAG and VCP via a common USB connection.

3.1.4 RAM, Flash

A 512MB or 1 GB LPDDR3 memory can be connected to the processor's DRAM interface via a 16-bit wide data bus. The memory clock is 533MHz, resulting in a DDR1-1066G 8-8-8 timing.

An eMMC is connected to the SDMMC2 interface of the processor via an 8-bit wide data bus. The signal level is fixed at 3.3V. This enables transfer modes up to DDR52. The default memory capacity is 8 GB. Other capacities can also be used by customizing the configuration.

A QSPI NOR flash with a memory capacity of 16 MiB is connected to the QUADSPI interface of the processor.

3.1.5 Power Supply

The module is supplied with 3.3 V via the SODIMM connector. This supplies all I/O interfaces on the module.

Two AP3445LW6 switching regulators from Diodes generate the voltages 1.21 V for the CPU core and 1.35 V for the DDR3L RAM on the module.

3.1.6 Display

The display is controlled via the LTDC interface of the processor. Two different display interfaces are supported:

- The RGB interface is routed to the SODIMM connector with 18 Bpp color depth and the associated sync signals HSYNC, VSYNC and DE.
- The DSI interface is routed to the SODIMM Extension 2 expansion connector. The assignment of the data and clock pairs correspond to the LVDS signals of the DIMM.MX53 and DIMM.MX6 modules. Both 18 Bpp and 24 Bpp color depth are possible on the DSI interface. Other signals, e.g. for controlling a touch controller integrated in the display, must be used by the SODIMM connection.

In addition to the color and sync signals, three other special signals for the display interfaces are available on the SODIMM connection:

- The LCD CLKI input on pin 68 of the SODIMM connector is connected to the processor pin I2S_CLK. This input can be used as a special, external source for the pixel clock of the LCD controller.
- The LCD_DON signal does not exist in the LCD controller of the processor. It is therefore realized via the GPIO PJ3. This can be used to switch a backlight on and off, for example.
- To control the backlight brightness, the PWM signal BL_CTRL is routed to pin 67 of the SODIMM connector. For this purpose, the GPIO PK1 of the processor is configured as PWM output TIM1_CH1.

The following assignment applies to the SODIMM connector:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
116	AUDIO_BCK	SAI1_SCK_A	PE5
47	LCD_D16	LTDC_R6	PA8
48	LCD_D17	LTDC_R7	PJ6
49	LCD_D14	LTDC_R4	PJ3
50	LCD_D15	LTDC_R5	PJ4
51	LCD_D12	LTDC_R2	PJ1
52	LCD_D13	LTDC_R3	PJ2
53	LCD_D10	LTDC_G6	PI1
54	LCD_D11	LTDC_G7	PK2
55	LCD_D8	LTDC_G4	PH15
56	LCD_D9	LTDC_G5	PH4
57	LCD_D6	LTDC_G2	PI15
58	LCD_D7	LTDC_G3	PJ12
59	LCD_D4	LTDC_B6	PK5
60	LCD_D5	LTDC_B7	PK6
61	LCD_D2	LTDC_B4	PK3
62	LCD_D3	LTDC_B5	PK4
63	LCD_D0	LTDC_B2	PJ14
64	LCD_D1	LTDC_B3	PD10
67	BL_CTRL	BL-PWM	PK1
68	LCD_LCLK	LTDC_LCLK	PI11
69	LCD_DISP	LTDC_DISP	PE13
70	LCD_DCK	LTDC_DCK	PE14
71	LCD_HSYN	LTDC_HSYNC	PI12
72	LCD_DON	GPIO	PJ3
73	LCD_VSYN	LTDC_VSYNC	PI13

3.1.7 Touch Interface

The TSC2003IPW component from Texas Instruments is used to control a resistive 4-wire touch sensor.

The device is connected to the I²C interface I2C1 and has the 7-bit address 0x48.

The pen interrupt goes to the GPIO PF2.

The following assignment applies to the SODIMM connector:

SODIMM Pin	SODIMM Signal
26	TOUCH_XP
28	TOUCH_XM
30	TOUCH_YP
32	TOUCH_YM

3.1.8 Camera, VIO0

A camera sensor is controlled via the DCMI interface of the processor. The interface is configured for an 8-bit data bus with external sync signals, in accordance with the SODIMM specification.

GPIO PI10 is output as signal VIO_RST# on pin91 of the SODIMM connector. The signal can trigger a reset on a camera.

The signals VIO_FLD, VIO_SRC and VIO_CKO of the SODIMM connector are not connected.

The following assignment applies to the SODIMM connector:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
78	VIO_D7	DCMI_D7	PI7
80	VIO_D6	DCMI_D6	PI6
82	VIO_D5	DCMI_D5	PD3
83	VIO_CLK	DCMI_PIXCLK	PC2
84	VIO_D4	DCMI_D4	PH14
85	VIO_HSYNC	DCMI_HSYNC	PH8
86	VIO_D3	DCMI_D3	PH12
87	VIO_VSYNC	DCMI_VSYNC	PI11
88	VIO_D2	DCMI_D2	PH11
90	VIO_D1	DCMI_D1	PH10
91	VIO_RST#	GPIO	PI10
92	VIO_D0	DCMI_D0	PH9

3.1.9 Audio

An external audio DAC is controlled via the SAI1 interface of the processor. The interface is configured as a master with clock out.

The following assignment applies to the SODIMM connector:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
116	AUDIO_BCK	SAI1_SCK_A	PE5
118	AUDIO_LRC	SAI1_FS_A	PG15
120	AUDIO_DATI	SAI1_SD_B	PF6
122	AUDIO_DATO	SAI1_SD_A	PD6
124	AUDIO_MCLK	SAI1_MCLK_A	PG7

3.1.10 Ethernet

The processor has a 10/100 MBit Ethernet interface ETH.

A PHY of type LAN8720A from Microchip is connected to the board via an RMII interface. The Ethernet transmit and receive lines go to the SODIMM connector.

The following applies to the PHY:

- The PHY has the MDIO address 0
- The interrupt output goes to GPIO PA6.
- A reset is triggered on the PHY via GPIO PA1 = 0.

The PHY's LED signals for link and traffic are routed to the SODIMM connector.

The following assignment applies to the SODIMM connector:

SODIMM Pin	SODIMM Signal
1	SPEED_LED#
3	TD_P
5	TD_N
9	RD_P
11	RD_N
13	LINK_LED#

3.1.11 USB Host, Device

The processor has a USB host interface with two channels and a USB OTG interface.

The USBH-1 interface is routed out as a host interface. As the processor has no dedicated control signals for a VBUS switch, this is realized via two GPIOs, PA10 serves as VBUS enable

output and PA11 as overcurrent input. Both lines are low-active and terminated with 10k pull-ups.

The USB-OTG interface is permanently configured as a USB device and routed out. Pin 10 of the SODIMM connector is connected to the OTG_VBUS pin of the processor. A VBUS power supply is not required.

The processor can boot via the USB device interface. This can be used to program the memory on board during production.

The following assignment applies to the SODIMM connector:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
2	USBH_PEN#	GPIO	PA10
4	USBH_OC#	GPIO	PA11
6	USBH_DN	USB_DM1	-
8	USBH_DP	USB_DP1	-
10	OTG_VBUS	OTG_VBUS	-
12	USBF_DN	USB_DM2	-
14	USBF_DP	USB_DP2	-

3.1.12 UARTs

There are five UART interfaces on the SODIMM connector:

- The UART-A interface has RS232 level and has the modem control signals RTS and CTS.
- The other four interfaces only have the data lines RxD, TxD and are available with LVTTTL level on the connector.
- In addition, there is the UART4 serial interface on the extended JTAG connector for debugging purposes.

The following applies to the assignment of the UARTs on the SODIMM connection:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
18	UART_A_TXD#	UART7 TxD	PE8
20	UART_A_RXD#	UART7 RxD	PE7
22	UART_A_RTS#	UART7 RTS	PE9
24	UART_A_CTS#	UART7 CTS	PE10.
21	UART_B_TXD	UART5 TX	PB13_.
23	UART_B_RXD	USRT5 RX	PB12
29	UART_C_TXD	USART1 TX	PA9
31	UART_C_RXD	USART1 RX	PB7
25	UART_D_TXD	USART2 TX	PD5
27	UART_D_RXD	USART2 RX	PF4
33	UART_E_TXD	USART3 TX	PC10
35	UART_E_RXD	USART3 RX	PD9

3.1.13 CAN

The CAN channel FDCAN1 is routed to pins 17 and 19 of the SODIMM connector as an LVTTTL signal. With a suitable external CAN transceiver, both a standard CAN interface and an FDCAN interface can be realized.

The following applies to the assignment of the CAN interface:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
17	CAN_TX	FDCAN1_TX	PH13
19	CAN_RX	FDCAN_RX	PI9

3.1.14 SDC Interface

The SDMMC1 interface of the processor is connected directly to the SODIMM connector. The signal level is fixed at 3.3V, which means that the maximum possible transfer rate is High Speed Mode at 50 MHz.

The following applies to the assignment of the SDC interface:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
96	SDC1_D0	SDMMC1_D0	PC8
98	SDC1_D1	SDMMC1_D1	PC9
100	SDC1_D2	SDMMC1_D2	PE6
102	SDC1_D3	SDMMC1_D3	PC11
104	SDC1_CMD	SDMMC1_CMD	PD2
106	SDC1_CLK	SDMMC1_CK	PC12
108	SDC1_CD#	MMC1_CD#	PG4
110	SDC1_WP#	GPIO	PF7

3.1.15 SPI

The SPI1 interface of the processor is led out on the SODIMM connector.

The following applies to the assignment of the SPI interface:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
111	SPI_SS#	SPI1-NSS#	PZ3
112	SPI-MISO	SPI1-MISO	PZ1
113	SPI-SCK	SPI1-SCK	PZ0
114	SPI-MOSI	SPI1-MOSI	PZ2

3.1.16 I2C

The I2C1 interface is connected to the SODIMM connector.

The following applies to the assignment of the I2C interface:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
115	SCL	I2C1-SCL	PD12
117	SDA	I2C1-SDA	PB9

The lines are terminated on the module with 2K2 pull-ups against 3.3V.

The TSC2003IPW touch controller is connected locally to the interface on the module. It occupies the address 0x48.

3.1.17 RTC

An RTC is integrated in the processor. The typical current consumption of the RTC is $\sim 1.25 \mu\text{A}$ at 25°C under the following conditions: retention RAM OFF, Backup SRAM OFF, RTC ON, LSE ON.

The RTC can be buffered via an external battery at the VBAT connection, pin 199 of the SODIMM connector.

3.1.18 Status LEDs

There are two status LEDs on the module. A red LED is connected to GPIO PA13, a green LED to PA14. The LEDs light up when the associated GPIO is low.

PA13 is controlled by the ROM loader of the processor to indicate boot errors. If booting is not possible, the red LED flashes. In engineering mode, the red LED is permanently on.

The green LED can be used by the software, e.g. as a heartbeat under Linux.

Signal	GPIO
LED_RED#	PA13
LED_GREEN#	PA14

3.1.19 Analog Inputs

Four analog signals are recorded on the module.

All inputs come from the SODIMM connector and are buffered by an OPAMP of type OPA4171 from Texas Instruments. The OPAMPs are wired as voltage followers and reduce the impedance of the inputs. All four signals are digitized by the ADC1 with 12-bit resolution.

The internal reference voltage of 2.5 V is used for the ADC, resulting in an input voltage range of 0- 2.5 V. Higher input voltages must be divided externally if necessary.

The following analog channels are used:

SODIMM Pin	SODIMM Signal	STM32MP157 Signal	GPIO
34	ANA1	ADC1_INP0	ANA0
36	ANA2	ADC1_INP1	ANA1
37	ANA4	ADC1_INP2	PF11
38	ANA3	ADC1_INP5	PB1

3.1.20 Digital GPIOs

The following GPIOs are individually connected to the SODIMM connector:

SODIMM Pin	SODIMM Signal	GPIO
125	GPIO8	PF12
126	GPIO9	PA0
127	GPIO6	PF14
128	GPIO7	PG5
129	GPIO4	PA5
130	GPIO5	PG10
131	GPIO2	PD0
132	GPIO3	PH2
133	GPIO0	PD1
134	GPIO1	PH6
184	IRQ1	PG3
186	IRQ2	PG8
188	IRQ3	PB8

3.1.21 Reset

Pin 192 of the SODIMM connector is the reset input of the module. The input is low active.

Pin 190 is a reset output with totem pole characteristic. The output is low while the reset input is active and can be driven to 0 by the software by setting GPIO PF3 to 0 for 240 ms.

4 Connectors

4.1 P1, SODIMM Connector

The SODIMM connection is implemented as a PCB edge connector that fits a 200-pin DDR2 SODIMM socket with 2.5 V keying.

An example of a counterpart is component 6-1473005-1 from TE.

Assignment of the SODIMM connection:

Pin	Signal	Signal	Pin
1	SPEED_LED#	USBH_PEN#	2
3	ETH_TDP	USBH_OC#	4
5	ETH_TDM	USBH_DM	6
7	GND	USBH_DP	8
9	ETH_RDP	USBF_VBUS	10
11	ETH_RDM	USBF_DM	12
13	LINK_LED	USBF_DP	14
15	n/c	GND	16
17	CAN_TX	UART-A_TXD#	18
19	CAN_RX	UART-A_RXD#	20
21	UART-E_TXD	UART-A_RTS#	22
23	UART-E_RXD	UART-A_CTS#	24
25	UART-D_TXD	Touch_XP	26
27	UART-D_RXD	Touch_XM	28
29	UART-C_TXD	Touch_YP	30
31	UART-C_RXD	Touch_YM	32
33	UART-B_TXD	ANA1	34
35	UART-B_RXD	ANA2	36
37	ANA4	ANA3	38
39	+3V3	GND	40
41	n/c	n/c	42
43	n/c	n/c	44
45	n/c	n/c	46
47	LCD_D16	LCD_D17	48
49	LCD_D14	LCD_D15	50
51	LCD_D12	LCD_D13	52
53	LCD_D10	LCD_D11	54
55	LCD_8	LCD_D9	56

Pin	Signal	Signal	Pin
57	LCD_D6	LCD_D7	58
59	LCD_D4	LCD_D5	60
61	LCD_D2	LCD_D3	62
63	LCD_D0	LCD_D1	64
65	+3V3	GND	66
67	BL_CTRL	LCD_LCLK	68
69	LCD_DISP	LCD_DCK	70
71	LCD_HSYN	LCD_DON	72
73	LCD_VSYN	n/c	74
75	n/c	n/c	76
77	n/c	VIO0_D7	78
79	n/c	VIO0_D7	80
81	n/c	VIO0_D7	82
83	VIO0_CLK	VIO0_D4	84
85	VIO0_HD	VIO0_D3	86
87	VIO0_VD	VIO0_D2	88
89	n/c	VIO0_D1	90
91	VIO_RST#	VIO0_D0	92
93	+3V3	GND	94
95	n/c	SDC1_D0	96
97	n/c	SDC1_D1	98
99	n/c	SDC1_D2	100
101	n/c	SDC1_D3	102
103	n/c	SDC1_CMD	104
105	n/c	SDC1_CLK	106
107	n/c	SDC1_CD#	108
109	n/c	SD1_WP#	110
111	SPI_SS#	SPI_MISO	112
113	SPI_SCK	SPI_MOSI	114
115	SCL	AUDIO_BCK	116
117	SDA	AUDIO_LRC	118
119	n/c	AUDIO_DATI	120
121	n/c	AUDIO_DATO	122
123	GND	AUDIO_MCLK	124
125	GPIO8	GPIO9	126

Pin	Signal	Signal	Pin
127	GPIO6	GPIO7	128
129	GPIO4	GPIO5	130
131	GPIO2	GPIO3	132
133	GPIO0	GPIO1	134
135	+3V3	GND	136
137	n/c	n/c	138
139	n/c	n/c	140
141	n/c	n/c	142
143	n/c	n/c	144
145	n/c	GND	146
147	n/c	n/c	148
149	n/c	n/c	150
151	n/c	n/c	152
153	n/c	n/c	154
155	n/c	n/c	156
157	n/c	n/c	158
159	n/c	n/c	160
161	+3V3	GND	162
163	n/c	n/c	164
165	n/c	n/c	166
167	n/c	n/c	168
169	n/c	n/c	170
171	n/c	n/c	172
173	n/c	n/c	174
175	n/c	n/c	176
177	n/c	n/c	178
179	n/c	n/c	180
181	n/c	n/c	182
183	n/c	IRQ_1	184
185	n/c	IRQ_2	186
187	n/c	IRQ_3	188
189	n/c	RESO#	190
191	n/c	RESI#	192
193	n/c	n/c	194
195	n/c	n/c	196

Pin	Signal	Signal	Pin
197	n/c	n/c	198
199	VBAT	GND	200

4.2 J2, SODIMM Extension2

The SODIMM Extension2 connector is a 30-pin connector 529910308 from Molex.

The counterpart on the baseboard is the type 537480308 from Molex.

Assignment of the SODIMM Extension2 connector:

Pin	Signal	Pin	Signal
1	n/c	2	n/c
3	n/c	4	n/c
5	n/c	6	DSI_TX0_N
7	n/c	8	DSI_TX0_P
9	GND	10	GND
11	n/c	12	DSI_TX1_N
13	n/c	14	DSI_TX1_P
15	n/c	16	GND
17	n/c	18	DSI_CLK_N
19	n/c	20	DSI_CLK_P
21	n/c	22	GND
23	n/c	24	n/c
25	n/c	26	n/c
27	n/c	28	GND
29	n/c	30	n/c

4.2.1 JP1, JTAG Connector

The JTAG connector is a 14-pin male connector with 1.27 mm pitch, in accordance with the STDC14 specification from ST Microelectronics.

Assignment of the JTAG connector:

Pin	Signal	Pin	Signal
1	n/c	2	n/c
3	Vcc	4	TMS/SWDIO
5	GND	6	TCK/SWCLK
7	GND	8	TDO/SWO
9	RCLK	10	TDI
11	GND	12	NRST
13	UART4-RxD	14	UART4-TxD

5 Technical Properties

5.1 Energy Supply

Power supply	3,3 V, +/-5%
Power consumption	tbd

5.2 Ambient Conditions

Working temperature range	-25 ... +70°C
Storage temperature range	-40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

5.3 Mechanical Specifications

Weight	approx. 17 g
Printed circuit board	Glas-Epoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 49.0 mm x 10.0 mm

6 Dimensional Drawing

