# emSTAMP-Argon
# emSBC-Argon

## Hardware Manual

including the emSTAMP-Argon processor module
and the emSBC-Argon development board

**Rev13 / 08.01.2024**

**emtrion GmbH**

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| Rev | Date/Signature | Changes |
|---|---|---|
| **0** | 25.07.2019/We | Preliminary revision |
| **1** | 30.09.2019/We | First revision including the emSBC-Argon |
| **2** | 04.02.2020/We | Added chapter 7.4.2 with recommended footprint |
| **3** | 21.02.2020/We | Update of temperature range in chapter 7.2 |
| **4** | 03.03.2020/We | Update of technical characteristics chapter 7 |
| **5** | 24.03.2020/We | Description of USBOTG_VBUS detection added to USB 2.0 OTG chapters. |
| **6** | 29.06.2020/Sch | Corrected pin description in chapter 6.15 |
| **7** | 10.07.2020/We | Corrected ref-clock speed for Ethernet-Phy in chapter 5.5 |
| **8** | 29.07.2020/We | Corrected port names in chapter 0 |
| **9** | 17.11.2020/We | Chapter for I2C-Bus updated for CPU-Module and SBC |
| **10** | 05.11.2021/We | Change of operating temperature in chapter 7.2.2.<br>Note for not included battery added in chapter 6.12. |
| **11** | 23.09.2022/Bue | Document correction, Pins 38 and 40 in chapter 6.7 swapped |
| **12** | 14.12.2022/Bue | Minimum input voltage and maximum current consumption updated in chapter 5.21 |
| **13** | 08.01.2024/Bue | VREF characteristics of ADC/DAC changed in chapter 5.14<br>Hint on red LED in parallel to the ADC input at connector J10, Pin 2 added in chapter 6.15 |

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# 1 Introduction

The emSTAMP-Argon processor module is a CPU board of emtrions emSTAMP-family, based on the STM32MP157 processor from STMicroelectronics. The STM32MP157 has an ARM Cortex-A7 dual-core and an ARM Cortex-M4.

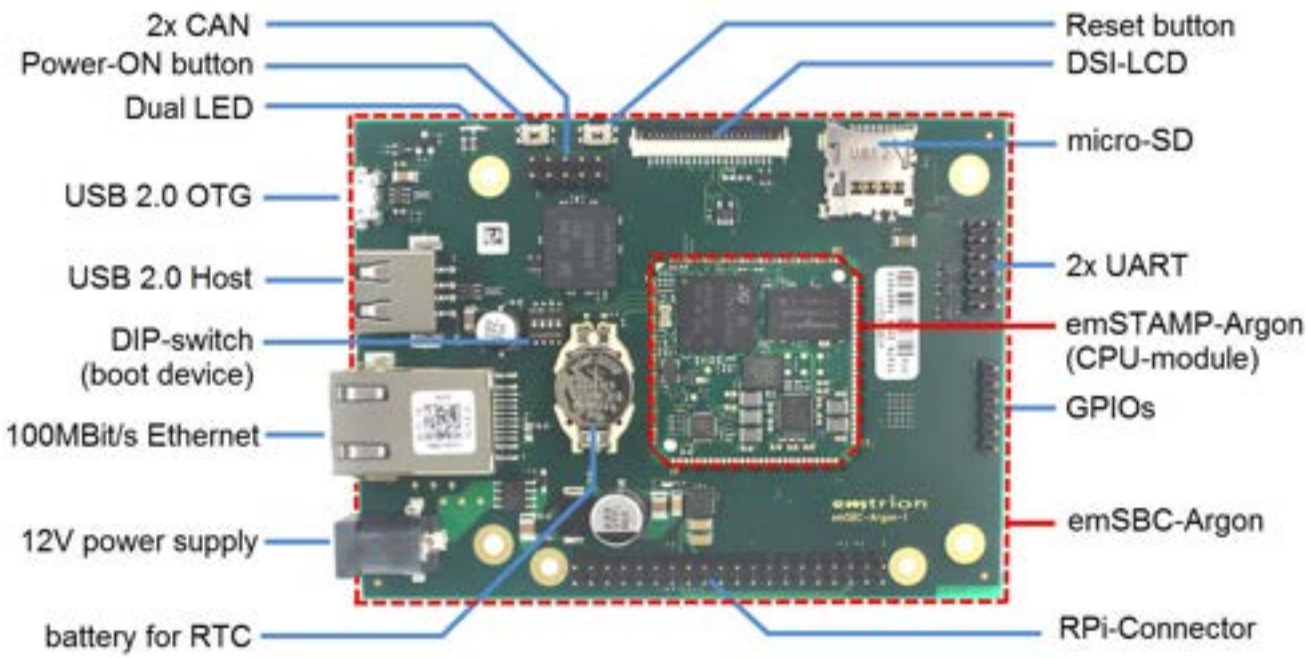
The dual-core Cortex-A7 may be clocked up to 650MHz and includes a variety of functions required for IOT, industrial or multimedia applications.

The CPU board is designed as a compact module with castellated mounting holes with 1.0mm pitch that can be soldered directly on a baseboard. As an extension the CPU board has additional solder pads on its bottom side which can be used if RGB- or JTAG-Interface are needed.

The emSBC-Argon development board is an SBC which is built around the CPU module. It provides direct access to a set of the module's interfaces. It is targeted to quickly start into product development.

The functionalities of the emSTAMP-Argon CPU board as well as the emSBC-Argon development board are both documented in this manual.

# 2 Overview of the emSBC-Argon with embedded emSTAMP-Argon

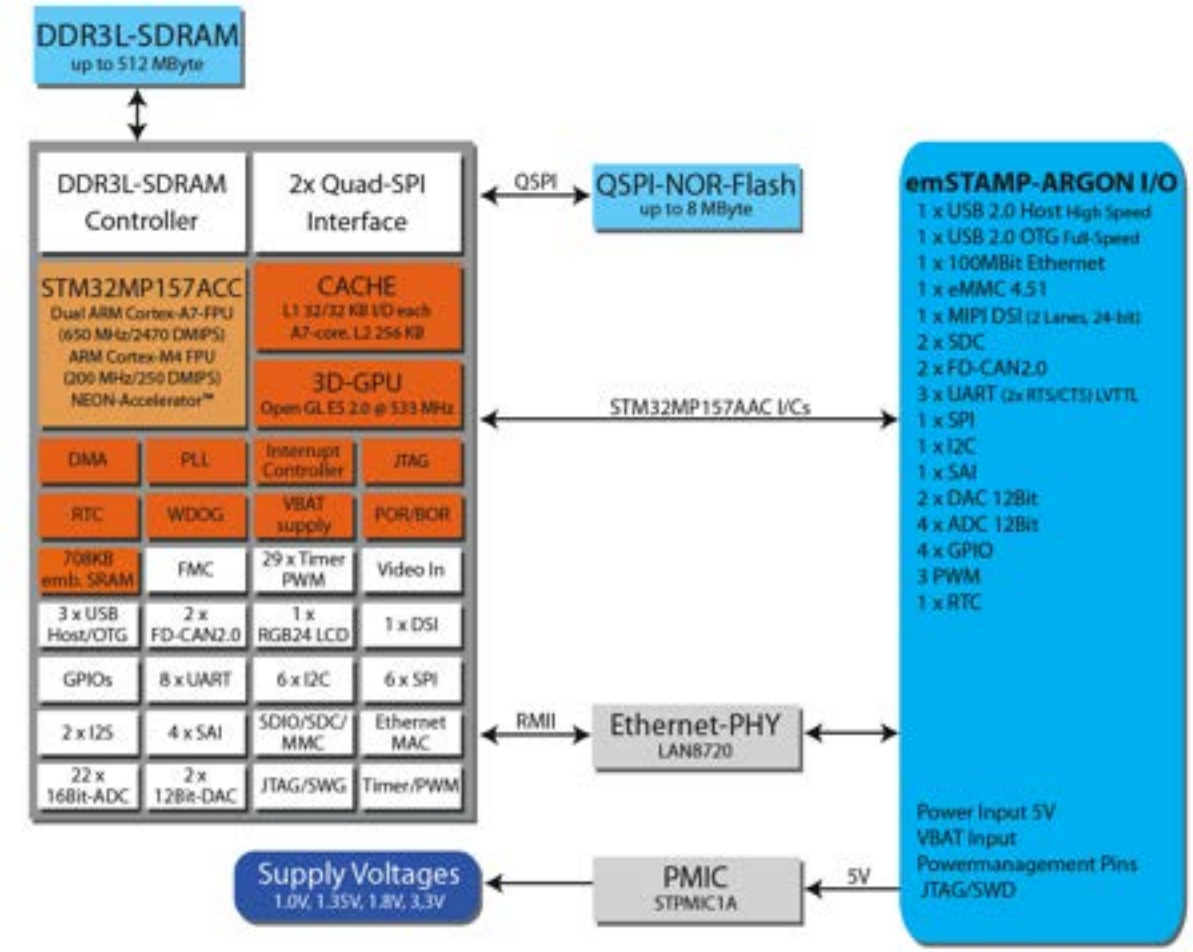


# 3 Handling Precautions

Please read the following notes prior to installing the processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The module does not need any configurations before installing
- The CPU module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Be sure all tools required for installation are electrostatic discharged as well.
- Handle the board with care and try to avoid touching its components or tracks.

# 4 Functional Overview of the CPU module (emSTAMP-Argon)




Block Diagram of the available Interfaces of the CPU module

# 5 Functional description of the CPU module (emSTAMP-Argon)

## 5.1 Processor

The emSTAMP-Argon CPU module uses the STM32MP157CAC processor from STMicroelectronics. The processor includes the ARM Cortex-A7 dual-cores (runs up to 650 MHz) and an ARM Cortex-M4 (runs up to 200 MHz). In addition to the CPU core, this processor provides a lot of features such as:

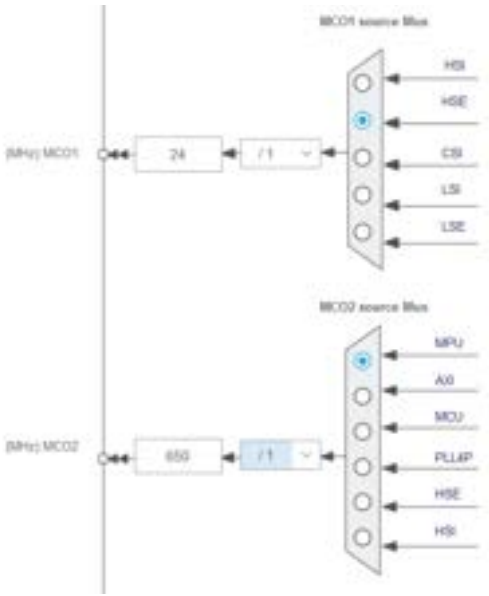
- Secure Boot, TrustZone, DES/TDES/AES cryptographic acceleration, Secure ROM and RAM
- NAND Flash controller (eMMC, SLC NAND-Flash)
- DDR3(L) SDRAM controller
- 3D GPU (OpenGL ES 2.0) with 133Mpix/sec @533MHz
- Ethernet MAC with 10/100 Mbit/s or 1Gbit/s
- 2 x USB 2.0 Host with high-speed mode
- USB 2.0 OTG with high-speed mode
- 3x SDMMC/SDIO controller
- LCD-TFT up to 24bpp and 1366x768 (WXGA) @60Hz
- 24 bit RGB interface TFT displays
- MIPI DSI with 2 data lanes each up to 1GHz
- 8- to 14-bit parallel camera interface
- 2x FDCAN controller
- serial interfaces:
  - 6 x $I^2C$
  - 6 x SPI
  - 8 x U(S)ART
  - 4 x SAI (stereo audio)
- Up to 29 Timer for encoder input, PWM output
- 2 x ADC (up to 16-bit resolution, up to 5Msps)
- 2 x DAC with 12-bit resolution and 1 MHz
- JTAG debug interface
- Real time clock

### 5.1.1 Processor Clocks

The processors high-speed external clock signal (HSE) is generated by an external 24MHz oscillator, which is connected to the HSE_OSC_IN pin. Several internal dividers and PLLs multiply the 24 MHz HSE input clock to the internal clocks. The SysClock is set to its maximum speed of 650 MHz.

A 32.768 KHz crystal is connected to the Low Speed External oscillator (LSE) of the processor. Its main application is to generate the clock for the processors RTC. The emSTAMP-Argon module has a dedicated pin for battery supply of the RTC block if the main power supply of the STM32MP157 is turned off.

The STM32MP157 has two pins for "Microcontroller Clock Output" (MCO1 and MCO2) which are connected to the castellated mounting holes. Each MCO has its own MUX and prescaler to select the clock source of the MCO1 and MCO2 (see picture below).




Pinout of MCO1 and MCO2 on the emSTAMP-Argon module:

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **72** | PG2 | RCC_MCO_2 | O | |
| **73** | PI11 | RCC_MCO_1 | O | |

More information about the STM32P157 clock system is described in the chapter 10 "Reset and Clock Control (RCC)" of the Reference manual from STMicroelectronics.

### 5.1.2 Boot Configuration

The STM32MP157 offers different boot modes which are selected by the three CPU pins BOOT[2:0]. The different boot modes which are available on the emSTAMP-Argon are shown in the table below:

| BOOT2 | BOOT1 | BOOT0 | Initial boot mode |
|---|---|---|---|
| 0 | 0 | 0 | UART and USB |
| 0 | 0 | 1 | QUADSPI NOR-Flash |
| 0 | 1 | 0 | eMMC on SDMMC2 (only fitted on SBC) |
| 1 | 0 | 1 | SD-Card on SDMMC1 |
| 1 | 1 | 0 | UART and USB |

On the emSTAMP-Argon module the three boot configuration pins BOOT[2:0] are connected to 1k pull-up resistor. The boot pins BOOT[2..0] are connected to the castellated mounting holes of the module. The desired boot mode has to be set by appropriate setting of these three boot pins on the carrier board.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **3** | BOOT0 | BOOT0 | I | PU 1K |
| **4** | BOOT1 | BOOT1 | I | PU 1K |
| **5** | BOOT2 | BOOT2 | I | PU 1K |

Note: The emSBC-Argon provides a DIP-switch to set the different boot modes. Please refer to chapter 6.11 “Boot configuration DIP-Switch” for details how to set the boot mode on the emSBC-Argon by the DIP-switch.

## 5.2 DDR3L SDRAM

The emSTAMP-Argon CPU module provides up to 512MiB DDR3L SDRAM as main memory. The RAM is connected via a 16 bit width data bus und may be clocked up to 533MHz.

## 5.3 QSPI-NOR Flash

A 16-Mibit QSPI-NOR flash memory (IS25LP016D form ISSI) is integrated on the CPU module. It is used to hold the initial Bootloader that provides the basic boot functionality of the module. The flash is connected to the QUAD-SPI bank1 with Quad-SPI-lines.

| Module Pin | CPU Pin Name | Signal |
|---|---|---|
| - | PF8 | QUADSPI_BK1_IO0 |
| - | PF9 | QUADSPI_BK1_IO1 |
| - | PF7 | QUADSPI_BK1_IO2 |
| - | PF6 | QUADSPI_BK1_IO3 |
| - | PB6 | QUADSPI_BK1_CS# |
| - | PF10 | QUADSPI_CLK |

Internal connection of QSPI-NOR-flash on the CPU-module

## 5.4 eMMC – NAND Flash interface

To store the operation system and application data, the CPU-module provides an eMMC-interface to connect a NAND-Flash to the emSTAMP-Argon. It is connected to the 8-bit SDMMC2 interface of the STM32MP157 and can be used a boot device.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **98** | PE3 | SDMMC2_CK | O | SR 22R |
| **99** | PG6 | SDMMC2_CMD | O | |
| **101** | PB14 | SDMMC2_D0 | I/O | |
| **102** | PB15 | SDMMC2_D1 | I/O | |
| **103** | PB3 | SDMMC2_D2 | I/O | |
| **104** | PB4 | SDMMC2_D3 | I/O | |
| **105** | PA8 | SDMMC2_D4 | I/O | |
| **106** | PA9 | SDMMC2_D5 | I/O | |
| **107** | PE5 | SDMMC2_D6 | I/O | |
| **108** | PC7 | SDMMC2_D7 | I/O | |
| **89** | PF14 | EMMC_RST# | O | |

The NAND Flash size can be between 4GB and 32GB depending on the ordering code.

Please contact emtrion GmbH for your required NAND Flash size.

## 5.5 Ethernet

The emSTAMP-Argon module provides an Ethernet interface with up to 100BASE-TX full duplex. The Ethernet MAC interface of the STM32MP157 CPU is connected in RMII mode to the external PHY LAN8720A from Microchip. The PHY address is set to 0.

A 50MHz clock is generated by the STM32MP157 on its ETH Clock Output (available at PB5) and connected to the XTAL1/CLKIN of the PHY.

The reset input nRST of the PHY is controlled via the PA1 of the STM32MP157. An external 10k pull-down resistor is connected to this signal to hold the PHY in reset during start-up of the CPU.

| Module Pin | CPU Pin Name | Signal |
|---|---|---|
| - | PC1 | ETH1_MDC |
| - | PA2 | ETH1_MDIO |
| - | PA7 | ETH1_CRS_DV |
| - | PC4 | ETH1_RXD0 |
| - | PC5 | ETH1_RXD1 |
| - | PB11 | ETH1_TX_EN |
| - | PG13 | ETH1_TXD0 |
| - | PG14 | ETH1_TXD1 |
| - | PB5 | ETH1_CLK |
| - | PA1 | ETH1_RESET# |

Internal connection of Ethernet-MAC interface on the CPU-module

The PHY LAN8720A is integrated on the CPU module so that an Ethernet Jack (with integrated magnetics) may be directly connected to the modules Ethernet pins ETH_RDP/ETH_RDM and ETH_TDP/ETH_TDM which are available at the castellated mounting holes of the module. An appropriate 1:1 transformer with a 100nF capacitor to GND and a 3.3V supply at each center tap pin must be added externally. Link or traffic indication signals for additional LEDs are not provided.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **19** | - | ETH_TDM | AO | |
| **20** | - | ETH_TDP | AO | |
| **22** | - | ETH_RDM | AI | |
| **23** | - | ETH_RDP | AI | |

## 5.6 USB 2.0

The STM32MP157 contains two high-speed PHYs. The processor provides an USB 2.0 high-speed host controller and an USB 2.0 OTG high-speed controller.

### 5.6.1 USB 2.0 Host

The STM32MP157 provides an USB 2.0 compliant host interface, supporting data transfers at low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) and high-speed (480Mbps). The VBUS supply voltage is provided by the PMIC of the emSTAMP-Argon. Over-current protection is done by the PMIC.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **50** | USB_DP1 | USBH_HS1_DP | AI/O | |
| **51** | USB_DM1 | USBH_HS1_DM | AI/O | |
| **52** | - | USBH VBUS | Power output | |

### 5.6.2 USB 2.0 OTG

The STM32MP157 provides an USB 2.0 compliant OTG interface, supporting data transfers at full-speed (12 Mbit/s) and high-speed (480Mbps).

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **40** | PA10 | USB_OTG_HS_ID | I | |
| **41** | OTG_VBUS (Pin AC19) | USBOTG_VBUS | Power I/O | |
| **43** | USB_DP2 | USB_OTG_HS_DP | AI/O | |
| **44** | USB_DM2 | USB_OTG_HS_DM | AI/O | |

If the USB_OTG_HS_ID signal (PA10) is tied to GND (logical “0”) by an external device/connector, the CPU module enters host mode. A floating ID signal places the CPU in device mode.

The VBUS supply voltage USBOTG_VBUS is provided by the PMIC of the emSTAMP-Argon and it is available at pin 41of the module. For VBUS detection, USBOTG_VBUS is also connected to the 5V-tolerant input OTG_VBUS (Pin AC19) of the processor.

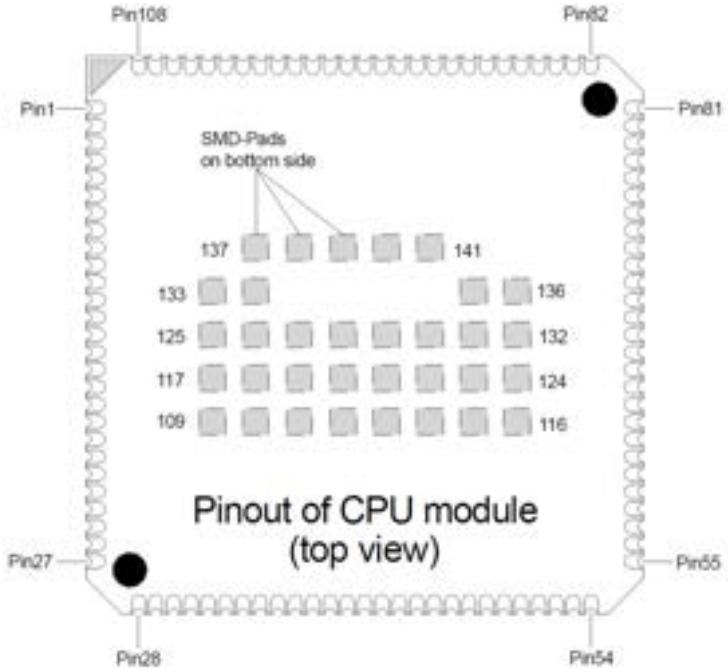
## 5.7 Display controller

The STM32MP157 provides two display controllers with different interfaces:

- a MIPI-DSI host controller with two data lanes
- a LCD-TFT display controller provides a 24-bit parallel digital RGB

The parallel 24-bit RGB-interface of LCD-TFT display controller has a special feature on the emSTAMP-Argon module. All pins 24-bit RGB interface are connected to SMD-pads on the bottom side of the module (see picture below).

The DSI-interface is connected to the castellated mounting holes on the edge of the module.




### 5.7.1 Display Serial Interface (DSI)

The MIPI-DSI-Interface of the STM32MP157 supports two data lanes with 1Gbit/s. The DSI controller supports color mapping of a16, 18 and 24-bit RGB. The pixel clock for the display data can be generated by an internal PLL. More information about the DSI interface of the STM32P157 system can be found in chapter 36 “DSI Host” of the Reference manual of STMicroelectronics.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **90** | DSI_D1P | DSI_D1_P | O | |
| **91** | DSI_D1N | DSI_D1_N | O | |
| **92** | - | GND | Power | |
| **93** | DSI_CKN | DSI_CLK_N | O | |
| **94** | DSI_CKP | DSI_CLK_P | O | |
| **95** | - | GND | Power | |
| **96** | DSI_D0P | DSI_D0_P | O | |
| **97** | DSI_D0N | DSI_D0_N | O | |

### 5.7.2 LCD-TFT display controller (LTDC)

The LCD-TFT display controller (LTDC) of the STM32MP157 provides a parallel RGB interface with up to 24-bit color (RGB-888). This interface supports a wide range of LCD- and TFT-panels with up to WXGA (1366 x 768) @ 60 fps. As control signals it provides V-Sync, H-Sync, pixel clock and data enable. The LTDC has two display layers each with 64 x 64-bit FIFO.

The following table shows the LTDC color output in RGB-888, RGB-666 and RGB-565 format. If less than 8-bit per color are used (RGB-666 and RGB-565), the RGB data lines of the LCD panel must be connected to the MSB of the LTDCs RGB data lines.

| LTDC on module | LCD RGB-888 | LCD RGB-666 | LCD RGB-565 |
|---|---|---|---|
| LTDC_B0 | LCD-B0 | | |
| LTDC_B1 | LCD-B1 | | |
| LTDC_B2 | LCD-B2 | LCD-B0 | |
| LTDC_B3 | LCD-B3 | LCD-B1 | LCD-B0 |
| LTDC_B4 | LCD-B4 | LCD-B2 | LCD-B1 |
| LTDC_B5 | LCD-B5 | LCD-B3 | LCD-B2 |
| LTDC_B6 | LCD-B6 | LCD-B4 | LCD-B3 |
| LTDC_B7 | LCD-B7 | LCD-B5 | LCD-B4 |
| LTDC_G0 | LCD-G0 | | |
| LTDC_G1 | LCD-G1 | | |
| LTDC_G2 | LCD-G2 | LCD-G0 | LCD-G0 |
| LTDC_G3 | LCD-G3 | LCD-G1 | LCD-G1 |
| LTDC_G4 | LCD-G4 | LCD-G2 | LCD-G2 |
| LTDC_G5 | LCD-G5 | LCD-G3 | LCD-G3 |
| LTDC_G6 | LCD-G6 | LCD-G4 | LCD-G4 |
| LTDC_G7 | LCD-G7 | LCD-G5 | LCD-G5 |
| LTDC_R0 | LCD-R0 | | |
| LTDC_R1 | LCD-R1 | | |
| LTDC_R2 | LCD-R2 | LCD-R0 | |
| LTDC_R3 | LCD-R3 | LCD-R1 | LCD-R0 |
| LTDC_R4 | LCD-R4 | LCD-R2 | LCD-R1 |
| LTDC_R5 | LCD-R5 | LCD-R3 | LCD-R2 |
| LTDC_R6 | LCD-R6 | LCD-R4 | LCD-R3 |
| LTDC_R7 | LCD-R7 | LCD-R5 | LCD-R4 |

The following table shows the available signals of the parallel 24-bit RGB interface. The pinout of the pins can be found in the chapter “Castellation Connector”.

| Signal | Description |
|---|---|
| LTDC_R[7..0] | 8-bit red color data |
| LTDC_G[7..0] | 8-bit green color data |
| LTDC_B[7..0] | 8-bit blue color data |
| LTDC_HSYNC | horizontal sync signal |
| LTDC_VSYNC | vertical sync signal |
| LTDC_CLK | Pixel clock |
| LTDC_DE | Data enable |

## 5.8 CAN-FD

The emSTAMP-Argon supports both CAN modules of the STM32MP157 (FDCAN1 and FDCAN2). Both are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **13** | PB13 | FDCAN2_TX | O | |
| **14** | PB12 | FDCAN2_RX | I | |
| **34** | PD1 | FDCAN1_TX | O | |
| **35** | PD0 | FDCAN1_RX | I | |

## 5.9 SD card interface

For the SD card interface the SDIO port (SDMMC1) of the STM32MP157 is used. The interface is 4-bit wide and compatible with the SD Memory Card Specification Version 3.01 SDR50.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| 56 | PB7 | SDMMC1_CD# | I | |
| 57 | PC11 | SDMMC1_D3 | I/O | |
| 58 | PC10 | SDMMC1_D2 | I/O | |
| 59 | PC9 | SDMMC1_D1 | I/O | |
| **60** | **PC8** | **SDMMC1_D0** | **I/O** | |
| **61** | **PD2** | **SDMMC1_CMD** | **O** | |
| **62** | **PC12** | **SDMMC1_CK** | **O** | |

The interface SDMMC1 can be used as boot device during SD card boot. Minimum set of required signals for SD card boot are in **bold.**

## 5.10 UART/USARTs

The emSTAMP-Argon provides 3 U(S)ART interfaces on its castellated mounting holes. The USART ports USART2 and USART3 are both implemented with CTS/RTS flow control. The UART4 port is used as UART interface without flow control. All ports are able to communicate at speeds up to 10Mbit/s.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **36** | PG11 | UART4_TX | O | |
| **37** | PB2 | UART4_RX | I | |
| **64** | PB10 | USART3_TX | O | |
| **65** | PD9 | USART3_RX | I | |
| **66** | PG8 | USART3_RTS | O | |
| **67** | PD11 | USART3_CTS | I | |
| **79** | PD3 | USART2_CTS | I | |
| **80** | PD4 | USART2_RTS | O | |
| **81** | PD6 | USART2_RX | I | |
| **82** | PD5 | USART2_TX | O | |

## 5.11 I²C Interface

Up to six I2C bus interface are available at the STM32MP157. The interfaces I2C1 and I2C5 are directly connected as LVTTL signals to the castellated mounting holes of the module. I2C4 is connected to the PMIC of the CPU module and not available on the castellation connector. The I2C interfaces and support standard (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s) and fast mode-plus (up to 1Mbit/s). They also support SMBus 2.0 and PMBus 1.1.

**Important note for carrier board design:**

At both I2C interfaces there are no pull-up resistors equipped on the emSTAMP-Argon module. The pull-up resistors have to be added on the carrier board.

On the CPU module there is one device connected to I2C4:

| Slave | Device | Chip-Address (7-bit) |
|---|---|---|
| PMIC | STPMIC1A | 0x33 |

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **75** | PA12 | I2C5_SDA | I/O | on carrier board |
| **76** | PA11 | I2C5_SCL | O | on carrier board |
| **77** | PF15 | I2C1_SDA | I/O | on carrier board |
| **78** | PD12 | I2C1_SCL | O | on carrier board |
| **Internal use** | PZ5 | I2C4_SDA | I/O | PU 1K5 |
| **Internal use** | PZ4 | I2C4_SCL | O | PU 1K5 |

## 5.12 SPI Interface

On the emSTAMP-Argon module the SPI1 interface is directly connected to the castellated mounting holes. SPI1 can communicate at up to 50Mbit/s.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **68** | PZ0 | SPI1_SCK | O | |
| **69** | PZ3 | SPI1_CS# | O | |
| **70** | PZ2 | SPI1_MOSI | O | |
| **71** | PZ1 | SPI1_MISO | I | |

## 5.13 Serial Audio Interface (SAI)

The STM32MP157 offers a serial audio interface (SAI) with two independent sub-blocks. The SAI supports audio protocols like I2S (LSB or MSB-justified), PCM/DSP, TDM, AC'97 and SPDIF (SPDIF only as transmitter. The SAI supports sampling frequencies up to 192 KHz. The data size may be 8, 10, 16, 20, 24 or 32bits.

On the emSTAMP-Argon module the SAI2 of the STM32MP157 is connected to the castellated mounting holes. A master clock output signal is also connected.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **45** | PF11 | SAI2_SD_B | I | |
| **46** | PI6 | SAI2_SD_A | O | |
| **47** | PI5 | SAI2_SCK_A | O | |
| **48** | PE0 | SAI2_MCLK_A | O | |
| **49** | PI7 | SAI2_FS_A | O | |

## 5.14 ADC and DAC

The emSTAMP-Argon module provides 3 pins on its castellated mounting holes which are dedicated for analog input and output functionality. The ADC and the DAC use the same reference voltage which can be supplied by the VREF+ pin of the CPU or taken from an internal reference source.

On the emSTAMP-Argon the VREF+ pin is open per default. Therefore, the internal reference source must be used. A connection of the VREF+ pin to the 3.3V supply is possible by adding a resistor.

### 5.14.1 Analog to Digital Converter (ADC)

The STM32MP157 provides two independent analog to digital converters with up to 16 bit resolution. The two ADCs can be configured to work in simultaneous or interleaved conversion mode.
ADC2 can also be used to monitor VBAT, internal DAC1, internal DAC2 and the internal temperature sensor.

| Module Pin | CPU Pin Name | Signal | alternative port function |
|---|---|---|---|
| **15** | PF12 | GPIO_1 | ADC1_INP6, ADC1_INN2 |
| **38** | PA5 | DAC1_OUT2 | ADC1_INP19, ADC1_INN18, ADC2_INP19, ADC2_INN1, |
| **39** | PA4 | DAC1_OUT1 | ADC1_INP18, ADC2_INP18 |

### 5.14.2 Digital to Analog Converter (DAC)

The DAC can be configured to run in 8- or 12-bit mode.

| Module Pin | CPU Pin Name | Signal |
|---|---|---|
| **38** | PA5 | DAC1_OUT2 |
| **39** | PA4 | DAC1_OUT1 |

## 5.15 GPIOs

The emSTAMP-Argon module offers 8 free to use GPIO[7..0], on its castellated mounting holes. GPIO[7..3] additionally offer PWM as alternative port function.

There are 5 more GPIO[12-8] which are used for control functions on the emSBC-Argon (see table below). On a new carrier board GPIO[12..8] can be used in a different way.

| Module Pin | CPU Pin Name | Signal | Used on emSBC-Argon as | Alternate port function |
|---|---|---|---|---|
| **16** | PE7 | GPIO_00 | | |
| **15** | PF12 | GPIO_01 | | ADC1_INP6, ADC1_INN2 |
| **88** | PE1 | GPIO_02 | | |
| **8** | PH14 | GPIO_03 | | TIM8_CH2N |
| **9** | PD13 | GPIO_04 | | TIM4_CH2 |
| **10** | PH11 | GPIO_05 | | TIM5_CH2 |
| **11** | PE9 | GPIO_06 | | TIM1_CH1 |
| **12** | PE8 | GPIO_07 | | TIM1_CH1N |
| **83** | PZ6 | GPIO_08 | MAC_EEPROM_WP# | |
| **84** | PC6 | GPIO_09 | DSI_TE | |
| **85** | PZ7 | GPIO_10 | DSI_RESET# | |
| **86** | PF2 | GPIO_11 | TOUCH_IRQ | |
| **87** | PA15 | GPIO_12 | BACKLIGHT_CTRL | TIM2_CH1 |

## 5.16 JTAG Debug

For programming and debugging the STM32MP157 offers two interfaces:

- Serial Wire Debug (SWD)
- JTAG Debug

Both interfaces are available via the same pins on the SMD pads on the bottom side of the module.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **137** | JTCK-SWCLK | JTCK_SWCLK | I | IPD |
| **138** | JTMS-SWDIO | JTMS_SWDIO | I | IPU |
| **139** | JTDI | JTDI | I | IPU |
| **140** | JTDO-TRACESWO | JTDO | O | IPU |
| **141** | NJTRST | JTRST# | I | IPU |

## 5.17 Status LEDs

A dual-color (red and green) status LED is placed on the CPU module. The LEDs are connected to the port pins of the CPU via series resistors.

The LEDs are turned on while the GPIO is set to high. The LEDs may be used as custom specific indicators.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| - | PA13 | LED_RED | n.a. | SR 100R |
| - | PA14 | LED_GREEN | n.a. | SR 100R |

## 5.18 User Power-On Key (PONKEY#)

The PONKEY# signal may be used to wake the PMIC (power management IC) from powersave states (OFF, STOP and STANDBY). The PONKEY# has an internal pull-up resistor in the PMIC and should be driven by open drain/collector outputs, or connected to GND through a switch. If unused, leave this pin open.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **7** | - | PONKEY# | I | IPU |

## 5.19 Reset

The STM32MP157 CPU has an internal power supply supervisor, which includes an integrated power-on-reset (POR) and a power-down reset (PDR). On the emSTAMP-Argon CPU module the POR and PDR circuitry is always enabled by setting the PDR_ON pin of the CPU to high. The emSTAMP-Argon module provides 2 pins with reset functionality on its castellated mounting holes:

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **17** | - | RESET_MICO# | I | PU 10K |
| **18** | PG0 | RESET_MOCI# | O | |

The emSTAMP-Argon module provides a RESET_MICO# pin (Module_In_Carrierboard_Out) on which an external reset signal may be applied to reset the CPU module. The RESET_MICO# Pin has an external pull-up resistor and should be driven by open drain/collector outputs, or connected to GND through a switch. If unused, leave this pin open.

The RESET-MOCI# pin (Module_Out_Carrierboard_In) of the module provides access to the onboard reset network. It might be used to reset peripherals on the baseboard while the CPU is also in reset state. The RESET-MOCI# signal uses LVTTL level and is active low. RESET_MOCI# can be controlled via the GPIO output pin PG0 of the STM32MP157.

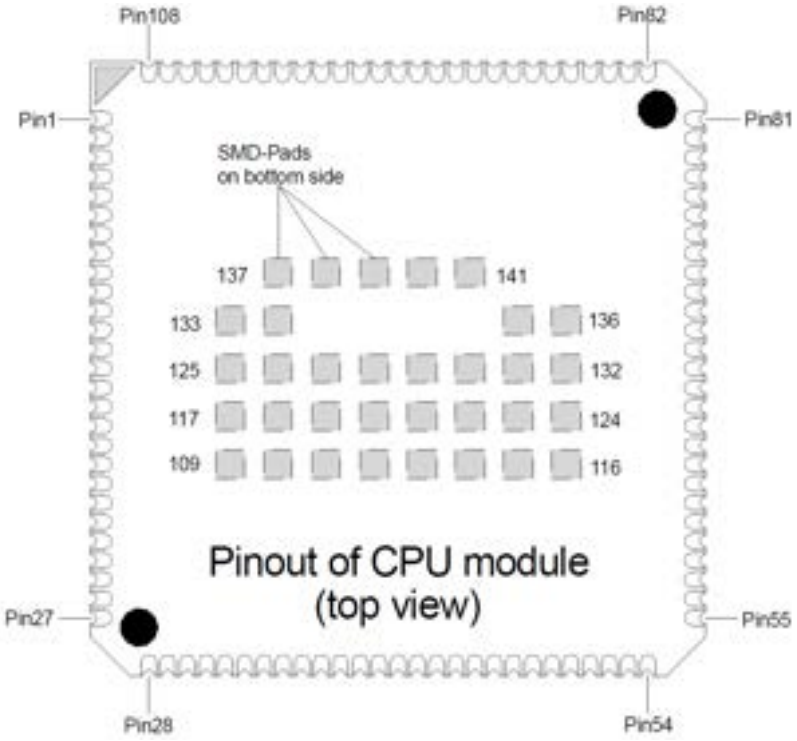
The RESET_MOCI# signal should never be driven by the user. Use the RESET_MICO# signal to provide an external reset.

## 5.20 Castellation Connector

For the placement and the orientation of the 108 castellated mounting holes of the emSTAMP-Argon module, please refer to chapter “Dimensional Drawing”.Abbreviations:

| | |
|---|---|
| AI | analogue input |
| AO | analogue output |
| I | digital input |
| O | digital output |
| I/O | digital bidirectional |

| | |
|---|---|
| PU xK | x KΩ pullup resistor |
| PD xK | x KΩ pulldown resistor |
| SR xR | x Ω series resistor |
| IPU xK | processor internal x KΩ pullup resistor |
| IPD xK | transistor internal x KΩ pulldown resistor |



In the following table the castellated mounting holes are referred to as **"Module Pins".** The "**CPU pin name"** refers to the STM32MP157 in the TFBGA-361 ball package.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **1** | - | +3V3 | Power output | |
| **2** | - | GND | Power | |
| **3** | BOOT0 | BOOT0 | I | PU 1K |
| **4** | BOOT1 | BOOT1 | I | PU 1K |
| **5** | BOOT2 | BOOT2 | I | PU 1K |
| **6** | VBAT | $V_{BAT}$ | Power input | |
| **7** | - | PONKEY# | I | IPU |
| **8** | PH14 | GPIO_03 (TIM8_CH2N) | I/O | |
| **9** | PD13 | GPIO_04 (TIM4_CH2) | I/O | |
| **10** | PH11 | GPIO_05 (TIM5_CH2) | I/O | |
| **11** | PE9 | GPIO_06 (TIM1_CH1) | I/O | |
| **12** | PE8 | GPIO_07 (TIM1_CH1N) | I/O | |
| **13** | PB13 | FDCAN2_TX | O | |
| **14** | PB12 | FDCAN2_RX | I | |
| **15** | PF12 | GPIO_01 | I/O | |
| **16** | PE7 | GPIO_00 | I/O | |
| **17** | - | RESET_MICO# | I | PU 10K |
| **18** | PG0 | RESET_MOCI# | O | |
| **19** | - | ETH_TDM | AO | |
| **20** | - | ETH_TDP | AO | |
| **21** | - | GND | Power | |
| **22** | - | ETH_RDM | AI | |
| **23** | - | ETH_RDP | AI | |
| **24** | - | GND | Power | |
| **25** | - | GND | Power | |
| **26** | - | GND | Power | |
| **27** | - | GND | Power | |
| **28** | - | $V_{IN}$ | Power input | |
| **29** | - | $V_{IN}$ | Power input | |
| **30** | - | $V_{IN}$ | Power input | |
| **31** | - | $V_{IN}$ | Power input | |
| **32** | - | $V_{IN}$ | Power input | |
| **33** | - | $V_{IN}$ | Power input | |
| **34** | PD1 | FDCAN1_TX | O | |
| **35** | PD0 | FDCAN1_RX | I | |
| **36** | PG11 | UART4_TX | O | |
| **37** | PB2 | UART4_RX | I | |
| **38** | PA5 | DAC1_OUT2 | O | |
| **39** | PA4 | DAC1_OUT1 | O | |
| **40** | PA10 | USB_OTG_HS_ID | I | |
| **41** | OTG_VBUS | USB_OTG VBUS | Power I/O | |
| **42** | - | GND | Power | |
| **43** | USB_DP2 | USB_OTG_HS_DP | AI/O | |
| **44** | USB_DM2 | USB_OTG_HS_DM | AI/O | |
| **45** | PF11 | SAI2_SD_B | I | |
| **46** | PI6 | SAI2_SD_A | O | |
| **47** | PI5 | SAI2_SCK_A | O | |
| **48** | PE0 | SAI2_MCLK_A | O | |
| **49** | PI7 | SAI2_FS_A | O | |
| **50** | USB_DP1 | USBH_HS1_DP | AI/O | |

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **51** | USB_DM1 | USBH_HS1_DM | AI/O | |
| **52** | - | USBH VBUS | Power output | |
| **53** | - | GND | Power | |
| **54** | - | +3V3 | Power output | |
| **55** | - | VDD_SD | Power output | |
| **56** | PB7 | SDMMC1_CD# | I | |
| **57** | PC11 | SDMMC1_D3 | I/O | |
| **58** | PC10 | SDMMC1_D2 | I/O | |
| **59** | PC9 | SDMMC1_D1 | I/O | |
| **60** | PC8 | SDMMC1_D0 | I/O | |
| **61** | PD2 | SDMMC1_CMD | O | |
| **62** | PC12 | SDMMC1_CK | O | |
| **63** | - | GND | Power | |
| **64** | PB10 | USART3_TX | O | |
| **65** | PD9 | USART3_RX | I | |
| **66** | PG8 | USART3_RTS | O | |
| **67** | PD11 | USART3_CTS | I | |
| **68** | PZ0 | SPI1_SCK | O | |
| **69** | PZ3 | SPI1_CS# | O | |
| **70** | PZ2 | SPI1_MOSI | O | |
| **71** | PZ1 | SPI1_MISO | I | |
| **72** | PG2 | RCC_MCO_2 | O | |
| **73** | PI11 | RCC_MCO_1 | O | |
| **74** | - | GND | Power | |
| **75** | PA12 | I2C5_SDA | I/O | |
| **76** | PA11 | I2C5_SCL | O | |
| **77** | PF15 | I2C1_SDA | I/O | |
| **78** | PD12 | I2C1_SCL | O | |
| **79** | PD3 | USART2_CTS | I | |
| **80** | PD4 | USART2_RTS | O | |
| **81** | PD6 | USART2_RX | I | |
| **82** | PD5 | USART2_TX | O | |
| **83** | PZ6 | GPIO_08 (MAC_EEPROM_WP#) | I/O | |
| **84** | PC6 | GPIO_09 (DSI_TE) | I/O | |
| **85** | PZ7 | GPIO_10 (DSI_RESET#) | I/O | |
| **86** | PF2 | GPIO_11 (TOUCH_IRQ) | I/O | |
| **87** | PA15 | GPIO_12 (BACKLIGHT_CTRL) | I/O | |
| **88** | PE1 | GPIO_02 | I/O | |
| **89** | PF14 | EMMC_RST# | O | |
| **90** | DSI_D1P | DSI_D1_P | O | |
| **91** | DSI_D1N | DSI_D1_N | O | |
| **92** | - | GND | Power | |
| **93** | DSI_CKN | DSI_CLK_N | O | |
| **94** | DSI_CKP | DSI_CLK_P | O | |
| **95** | - | GND | Power | |
| **96** | DSI_D0P | DSI_D0_P | O | |
| **97** | DSI_D0N | DSI_D0_N | O | |
| **98** | PE3 | SDMMC2_CK | O | SR 22R |
| **99** | PG6 | SDMMC2_CMD | O | |
| **100** | - | GND | Power | |

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **101** | PB14 | SDMMC2_D0 | I/O | |
| **102** | PB15 | SDMMC2_D1 | I/O | |
| **103** | PB3 | SDMMC2_D2 | I/O | |
| **104** | PB4 | SDMMC2_D3 | I/O | |
| **105** | PA8 | SDMMC2_D4 | I/O | |
| **106** | PA9 | SDMMC2_D5 | I/O | |
| **107** | PE5 | SDMMC2_D6 | I/O | |
| **108** | PC7 | SDMMC2_D7 | I/O | |

The following table shows the pinout of the SMD-Pads on the bottom side of the emSTAMP-Argon CPU module:

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **109** | PE4 | LTDC_B0 | O | |
| **110** | PG12 | LTDC_B1 | O | |
| **111** | PG10 | LTDC_B2 | O | |
| **112** | PD10 | LTDC_B3 | O | |
| **113** | PI4 | LTDC_B4 | O | |
| **114** | PA3 | LTDC_B5 | O | |
| **115** | PB8 | LTDC_B6 | O | |
| **116** | PD8 | LTDC_B7 | O | |
| **117** | PB1 | LTDC_G0 | O | |
| **118** | PB0 | LTDC_G1 | O | |
| **119** | PH13 | LTDC_G2 | O | |
| **120** | PE11 | LTDC_G3 | O | |
| **121** | PH15 | LTDC_G4 | O | |
| **122** | PI0 | LTDC_G5 | O | |
| **123** | PI1 | LTDC_G6 | O | |
| **124** | PI2 | LTDC_G7 | O | |
| **125** | PH2 | LTDC_R0 | O | |
| **126** | PH3 | LTDC_R1 | O | |
| **127** | PH8 | LTDC_R2 | O | |
| **128** | PH9 | LTDC_R3 | O | |
| **129** | PH10 | LTDC_R4 | O | |
| **130** | PC0 | LTDC_R5 | O | |
| **131** | PH12 | LTDC_R6 | O | |
| **132** | PE15 | LTDC_R7 | O | |
| **133** | PI10 | LTDC_HSYNC | O | |
| **134** | PI9 | LTDC_VSYNC | O | |
| **135** | PG7 | LTDC_CLK | O | |
| **136** | PE13 | LTDC_DE | O | |
| **137** | JTCK-SWCLK | JTCK_SWCLK | I | IPD |
| **138** | JTMS-SWDIO | JTMS_SWDIO | I | IPU |
| **139** | JTDI | JTDI | I | IPU |
| **140** | JTDO-TRACESWO | JTDO | O | IPU |
| **141** | NJTRST | JTRST# | I | IPU |

## 5.21 Power Supply

| Supply | Direction | $V_{min}$ | $V_{typ}$ | $V_{max}$ | Max. Current |
|---|---|---|---|---|---|
| **$V_{IN}$** | to module | 3.6V | 5.0V | 5.25V | 320 mA @ 5.0V [1] |
| **$V_{BAT}$** | to module | 1.2V | | 3.60V | 10 µA [2] |
| **+3V3** | from module | | 3.3V | | 1000 mA |
| **VDD_SD** | from module | | 3.3V | | 350 mA |
| **USBH_VBUS** | from module | 4.75V | 5.0V | 5.25V | 500 mA |
| **USB_OTG VBUS** | to/from module | 4.75V | 5.0V | 5.25V | 500 mA |

[1] Max. current while running "stress --cpu 2 --io 2 --vm 2 --vm-bytes 128M" under Linux
[2] RTC is on, LSE oscillator is on, Backup SRAM is off,

### 5.21.1 $V_{IN}$ Supply

The Module can be powered by a single supply between 3.6V and 5.25V. No additional supplies are required to use the basic functionality of the module.

### 5.21.2 VBAT Supply

The VBAT power domain contains the RTC, the backup registers, the retention RAM and the backup SRAM. Current consumption from the VBAT source (e.g. 3V lithium coin battery) with active RTC and LSE oscillator is typically below 10µA at 25°C ambient temperature.

### 5.21.3 +3V3 Supply

The +3V3 is generated on the module and can be used on the by the peripheral on the carrier board.

### 5.21.4 VDD_SD

VDD_SDMMC is the supply voltage for the SD-Card interface on the carrier board. It is internally connected to +3V3.

### 5.21.5 USBH_VBUS

USBH_VBUS is the 5.0V VBUS-voltage which is generated on the PMIC of the module. It has a current sense and provides over current protection at 600mA. USBH_VBUS can be directly connected to a USB Type-A connector (ESD protection, e.g. TVS-diodes, has to be added on the carrier board).

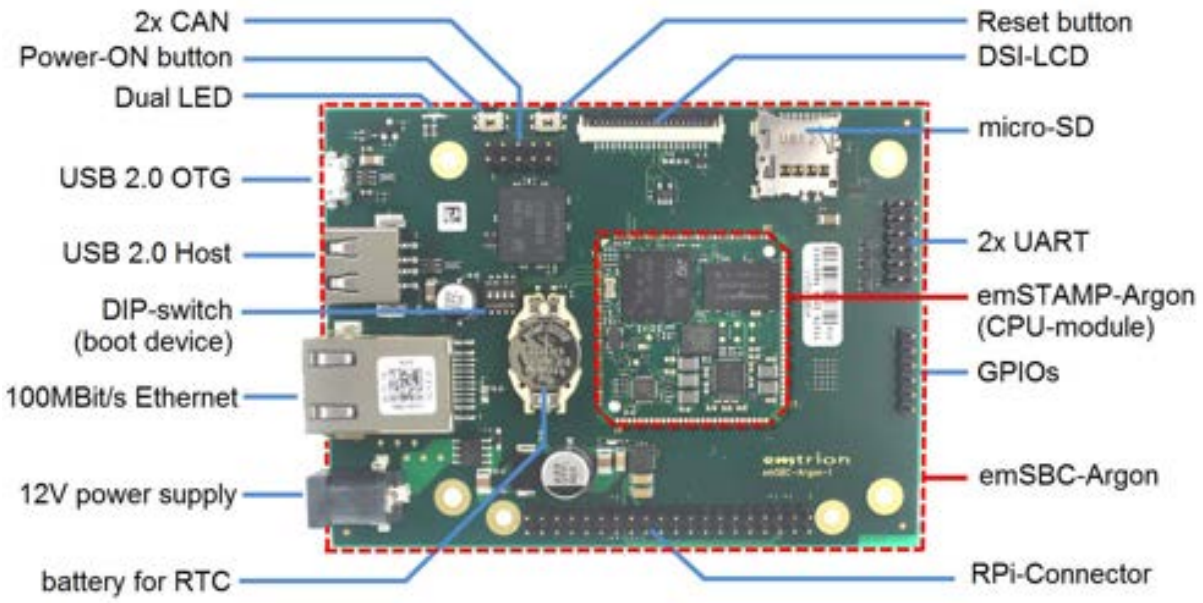
### 5.21.6 USB_OTG_VBUS

USB_OTG_VBUS is the 5.0V VBUS-voltage which is generated on the PMIC of the module. It has a current sense and provides over current protection at 600mA.

Depending of the USB_OTG_HS_ID signal (PA10) the emSTAMP-Argon module enters the host or the device mode:

- In host mode USB_OTG_VBUS is turned on and can supply the connected device.
- In device mode USB_OTH_VBUS is turned off. VBUS is supplied by the connected Host.

# 6 Functional Description of the Single-Board-Computer (emSBC-Argon)




## 6.1 eMMC NAND-Flash

To store the operating system and application data, an eMMC NAND Flash is provided on the emSBC-Argon board. It is connected to the SDMMC2 interface of the STM32MP157 processor. The NAND Flash size can be between 4GB and 32GB depending on the ordering code.

| Please contact emtrion GmbH for your required NAND Flash size. |
|---|

The onboard eMMC device can be reset either by the global reset signal RESET_MOCI# or by the EMMC_RST# signal at GPIO-PF14. At the STM32MP157 the GPIO-PF14 is configured as output. A low of the signal EMMC_RST# resets the eMMC-NAND Flash device.

The eMMC-device can also be used as boot-device. Please refer to the chapter 6.11 "Boot configuration DIP-Switch" for more information how to set the appropriate boot-configuration.

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **101** | PB14 | SDMMC2_D0 | I/O | |
| **102** | PB15 | SDMMC2_D1 | I/O | |
| **103** | PB3 | SDMMC2_D2 | I/O | |
| **104** | PB4 | SDMMC2_D3 | I/O | |
| **105** | PA8 | SDMMC2_D4 | I/O | |
| **106** | PA9 | SDMMC2_D5 | I/O | |
| **107** | PE5 | SDMMC2_D6 | I/O | |
| **108** | PC7 | SDMMC2_D7 | I/O | |
| **98** | PE3 | SDMMC2_CK | O | PU 10k |
| **99** | PG6 | SDMMC2_CMD | O | PU 4k7 |
| **89** | PF14 | EMMC_RST# | O | |

## 6.2 microSD-Card socket

A microSD-Card socket J6 is available on the emSBC-Argon. The socket J6 is connected to the SDMMC1 interface of the STM32MP157 processor via an integrated EMI-filter and TVS diodes array. An active-low card-detect signal of the microSD-Card socket is available but there is no write protection.

The microSD-Card socket can be used as boot-device. Please refer to the chapter 6.11 "Boot configuration DIP-Switch" for more information how to set the appropriate boot-configuration.

If the SDMMC1 interface needs to be available on the RPi-extension connector, these resistors need to be removed to avoid signal reflections caused by wire stubs.

### 6.2.1 Pinout of microSD-Card connector J6

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **1** | SDMMC1_D2 | PC10 | 58 |
| **2** | SDMMC1_D3 | PC11 | 57 |
| **3** | SDMMC1_CMD | PD2 | 61 |
| **4** | VDD_SD | | |
| **5** | SDMMC1_CK | PC12 | 62 |
| **6** | GND | | |
| **7** | SDMMC1_D0 | PC8 | 60 |
| **8** | SDMMC1_D1 | PC9 | 59 |
| **9** | SDMMC1_CD# | PB7 | 56 |
| **10** | GND | | |

**Note:** The SDMMC1 interface of the STM32MP157 is shared between the MicroSD-Card socket and the 40-pin RPi-extension connector J13. As default the SDMMC1 interface is connected to the microSD-Card socket via the 0R-resistors R66, R67, R68, R70, R71 and R72.

## 6.3 Ethernet Connector

A 10/100 MBit Ethernet interface is available via the RJ45 jack J9. The jack has an integrated magnetic whose DC level has to be connected to 3.3V.

LEDs for link status and transfer speed are not provided by the emSTAMP-Argon module.

### 6.3.1 Pinout ethernet connector J9

Type: HR961160C from manufacturer HanRun

| Pin | Signal | Module Pin |
|---|---|---|
| **1** | n.c. | |
| **2** | n.c. | |
| **3** | ETH_TDP | 20 |
| **4** | ETH_TDM | 19 |
| **5** | 3V3 | |
| **6** | 3V3 | |
| **7** | ETH_RDP | 23 |
| **8** | ETH_RDM | 22 |
| **9** | n.c. | |
| **10** | GND | |
| **11** | n.c. | |
| **12** | n.c. | |

## 6.4 DSI-LCD

The emSBC-Argon is equipped with the 20-pin FPC connector J3 to connect a TFT-LCD to the MIPI-DSI interface of the STM32MP157. The FPC connector has 1.0mm pitch and its type is bottom contact.

Both LCD-Boards available from ST-Microelectrioncs (**MB1407** and **B-LCD40-DSI1**) can be used by this FPC connector. These LCD-Boards have a 4-inch display, 480x800 resolution, 24bpp color depth and a capacitive touch.

### 6.4.1 Usage of LCD-Board MB1407

The pinout of FPC-connector J3 is compatible to the LCD-board **MB1407** of the STM32MP157-Discovery kits.

**Note:** for the connection of MB1407 a FPC-cable with top contacts on one side, and bottom on the other side has to be used (e.g. 686720100001 from Wuerth Electronics).

### 6.4.2 Usage of LCD-Board B-LCD40-DSI1

The developer kit of the emSBC-Argon-1 has a **B-LCD40-DSI1**-board from STMicroelectronics connected to its FPC-connector J3. For the connection of the B-LCD40-DSI1 a DSI-adapter-board needs to be used (see picture below).

Connecting the B-LCD40-DSI Display (STMicroelectronics) via the DSI-adapter board

### 6.4.3 Pinout of DSI-Connector J3

Type: 686120148922 from Wuerth Electronics

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **1** | GPIO_10 (DSI_RESET#) | PZ7 | 85 |
| **2** | GPIO_12 (BACKLIGHT_CTRL) | PA15 | 87 |
| **3** | GPIO_09 (DSI_TE) | PC6 | 84 |
| **4** | GPIO_11 (TOUCH_IRQ) | PF2 | 86 |
| **5** | GND | | |
| **6** | 3V3 | | |
| **7** | 3V3 | | |
| **8** | GND | | |
| **9** | I2C1_SDA | PF15 | 77 |
| **10** | I2C1_SCL | PD12 | 78 |
| **11** | GND | | |
| **12** | DSI_D0_P | DSI_D0P | 96 |
| **13** | DSI_D0_N | DSI_D0N | 97 |
| **14** | GND | | |
| **15** | DSI_CLK_P | DSI_CKP | 94 |
| **16** | DSI_CLK_N | DSI_CKN | 93 |
| **17** | GND | | |
| **18** | DSI_D1_P | DSI_D1P | 90 |
| **19** | DSI_D1_N | DSI_D1N | 91 |
| **20** | GND | | |

## 6.5 USB 2.0 HOST

The USB Host interface of the CPU board is connected to the USB Type-A connector J12. The used EMC filters are dimensioned for High Speed Mode with 480 MHz.

The VBUS output of the USB Host connector is provided by PMIC of the emSBC-Argon module. The VBUS supply voltage USBH_VBUS is available at pin 52 of the module and can provide up to 5W.

### 6.5.1 Connector USB 2.0 Host J12

Type: USB-A connector

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **1** | USBH VBUS | | 52 |
| **2** | USBH_HS1_DM | USB_DM1 | 51 |
| **3** | USBH_HS1_DP | USB_DP1 | 50 |
| **4** | GND | | 53 |

## 6.6 USB 2.0 OTG

A USB Host/Device interface is available at the micro-USB-AB connector J1. The used EMC filters are dimensioned for High Speed Mode with 480MHz.

The emSBC-Argon-1 is equipped with a reverse current protection at the VBUS-pin of micro-USB connector. This prevents current to flow into the USBOTG_VBUS-pin of the STM32MP157 processor if the module is in power down mode.

The VBUS output of the micro-USB-AB connector is provided by PMIC of the emSBC-Argon module. The VBUS supply voltage USBOTG_VBUS is available at pin 41 of the module and can provide up to 5W. For VBUS detection, USBOTG_VBUS is also connected to the 5V-tolerant input OTG_VBUS (Pin AC19) of the processor.

The interface of the CPU module must be configured according to the level of the ID pin. The STM32MP157 gets an OTG B-device (Client respectively Device) if nothing or a mini USB-B OTG connector is plugged in (ID pin is floating). With a plugged mini USB-A OTG connector (ID pin pulled to GND) the CPU gets an OTG A-device (Host) and supplies the VBUS Pin.

### 6.6.1 Pinout USB-OTG Connector J1

Type: micro-USB-AB

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **1** | USB_OTG VBUS | OTG_VBUS (Pin AC19) | 41 |
| **2** | USB_OTG_HS_DM | USB_DM2 | 44 |
| **3** | USB_OTG_HS_DP | USB_DP2 | 43 |
| **4** | USB_OTG_HS_ID | PA10 | 40 |
| **5** | GND | | 42 |

## 6.7 RPi Connector

The GPIO extension connector J13 is a dual-row pinheader with 40 pins with 100mil pitch. This GPIO expansion connector offers Raspberry Pi® shields capability.

The following interfaces of the STM32MP157 are provided on the extension connector:

- I2C1 and I2C5
- USART3 (with RTS/CTS)
- SPI1
- SDMMC1(see note below)
- SAI2
- MCO1 and MCO2 (Microcontroller Clock Output)
- GPIOs with PWM functionality as alternative port function

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **1** | 3.3V | | |
| **3** | I2C5_SDA | PA12 | 75 |
| **5** | I2C5_SCL | PA11 | 76 |
| **7** | RCC_MCO_1 | PI11 | 73 |
| **9** | GND | | |
| **11** | USART3_RTS | PG8 | 66 |
| **13** | SDMMC1_D3 | PC11 | 57 |
| **15** | SDMMC1_CK | PC12 | 62 |
| **17** | 3.3V | | |
| **19** | SPI1_MOSI | PZ2 | 70 |
| **21** | SPI1_MISO | PZ1 | 71 |
| **23** | SPI1_SCK | PZ0 | 68 |
| **25** | GND | | |
| **27** | I2C1_SDA | PF15 | 77 |
| **29** | RCC_MCO_2 | PG2 | 72 |
| **31** | TIM5_CH2 | PH11 | 10 |
| **33** | TIM8_CH2N | PH14 | 8 |
| **35** | SAI2_FS_A | PI7 | 49 |
| **37** | SDMMC1_D2 | PC10 | 58 |
| **39** | GND | | |

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **2** | 5.0V | | |
| **4** | 5.0V | | |
| **6** | GND | | |
| **8** | USART3_TX | PB10 | 64 |
| **10** | USART3_RX | PD9 | 65 |
| **12** | SAI2_SCK_A | PI5 | 47 |
| **14** | GND | | |
| **16** | SDMMC1_CMD | PD2 | 61 |
| **18** | SDMMC1_D0 | PC8 | 60 |
| **20** | GND | | |
| **22** | SDMMC1_D1 | PC9 | 59 |
| **24** | SPI1_CS# | PZ3 | 69 |
| **26** | GPIO_02 | PE1 | 88 |
| **28** | I2C1_SCL | PD12 | 78 |
| **30** | GND | | |
| **32** | TIM4_CH2 | PD13 | 9 |
| **34** | GND | | |
| **36** | USART3_CTS | PD11 | 67 |
| **38** | SAI2_SD_B | PF11 | 45 |
| **40** | SAI2_SD_A | PI6 | 46 |

**Note:** The SDMMC1 interface of the STM32MP157 is shared between the MicroSD-Card socket and the 40-pin RPi-extension connector J13. To be able to use the SDMMC1 interface at the RPi-extension connector:

- remove R66, R67, R68, R70, R71 and R72
- place 0R-resistors R9-R14

## 6.8 FD-CAN Connector

The two FDCAN interfaces (FDCAN1 and FDCAN2) of the STM32MP157 are directly connected to the dual-row pinheader J7 with 10 pins in 100mil pitch.

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| 1 | 3.3V | | |
| 2 | 3.3V | | |
| 3 | GND | | |
| 4 | GND | | |
| 5 | FDCAN1_TX | PD1 | 34 |
| 6 | FDCAN2_TX | PB13 | 13 |
| 7 | FDCAN1_RX | PD0 | 35 |
| 8 | FDCAN2_RX | PB12 | 14 |
| 9 | n.c. | | |
| 10 | n.c. | | |

## 6.9 UART connector

The emSBC-Argon provides USART2 (with RTS/CTS) and UART4 at the dual-row pinheader J4 with 12 pins in 100mil pitch.

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| 1 | GND | | |
| 2 | GND | | |
| 3 | USART2_RTS | PD4 | 80 |
| 4 | n.c. | | |
| 5 | n.c. | | |
| 6 | n.c. | | |
| 7 | USART2_RX | PD6 | 81 |
| 8 | UART4_RX | PB2 | 37 |
| 9 | USART2_TX | PD5 | 82 |
| 10 | UART4_TX | PG11 | 36 |
| 11 | USART2_CTS | PD3 | 79 |
| 12 | n.c. | | |

## 6.10 Reset & Wake-up Buttons

### 6.10.1 Reset Button S2

The push-button S2 is used to generate a reset to the STM32MP157 processor and the peripherals on the SBC.

The push-button S2 is connected to the RESET_MICO signal at pin-17 of the emSTAMP-Argon module. By pressing S2 the RESET_MICO signal is pulled low. The RESET_MICO signal has a 10k pull-up resistor which is equipped on the emSTAMP-Argon module.

### 6.10.2 Wake-up Button S1

The push-button S1 is directly connected with the active-low input PONKEY# of the PMIC (Power-Management-IC) on the emSTAMP-Argon module.

The pressed button S1pulls the signal PONKEY# low.

- This generates a SYS_WKUP signal at PA0 of the STM32MP157.
- Wakes up the PMIC from any low-power mode.

## 6.11 Boot configuration DIP-Switch

The DIP-switch SW1 is used to set the boot mode of the emSTAMP-Argon module. The BOOT[2:0] configuration pins are connected to SW1.

- If a switch is in position "ON", the corresponding pin is read as "0".
- If a switch is in position "OFF", the corresponding pin is read as "1".

The following table describes the available boot mode options:

| SW1-4 | SW1-3 | SW1-2 | SW1-1 | Initial boot mode |
|---|---|---|---|---|
| - | ON | ON | ON | UART and USB |
| - | ON | ON | OFF | QUADSPI NOR-Flash |
| - | ON | OFF | ON | eMMC on SDMMC2 |
| - | OFF | ON | OFF | SD-Card on SDMMC1 |
| - | OFF | OFF | ON | UART and USB |

Note: Switch SW1-4 is not connected.

## 6.12 Battery holder

A battery holder J11 for an CR1225 lithium coin cell is available to supply the VBAT power domain of the emSTAMP-Argon module. The VBAT power domain contains the RTC, backup registers, retention RAM and the backup SRAM of the STM32MP157 processor.

The battery holder J11 is connected via a 1k-resistor and a reverse-current-protection-diode to the VBAT-pin of the emSTAMP-Argon module:

| Module Pin | CPU Pin Name | Signal | Direction (module view ) | Termination |
|---|---|---|---|---|
| **6** | VBAT | $V_{BAT}$ | Power input | |

**Note:** Due to the current guidelines for the transport of batteries, the CR1225 lithium coin cell is not included.

## 6.13 I²C-Bus

On the emSBC-Argon there are two I²C- Busses available I2C1 and I2C5. Both I²C busses are terminated with 1k5-Pullup resistors on the emSBC-Argon board.

### 6.13.1 I2C1

On the emSBC-Argon there is one I²C device connected to I2C1. The device has three separate I2C-adresses:

| Slave | Device | Chip-Address (7-bit) |
|---|---|---|
| 2K-EEPROM | AT24MAC402 | 0x50 |
| extended memory block | AT24MAC402 | 0x58 |
| Write-Protect registers | AT24MAC402 | 0x30 |

The I2C1-Bus is also connected to the touch controller of the DSI-Display connector (see chapter 6.4.3 Pinout of DSI-Connector J3 for details) and to the RPi compatible connector (see chapter 6.7 for details).

### 6.13.2 I2C5

There are no I²C-devices connected to the I2C5-Bus on the emSBC-Argon. The I2C5-Bus is only connected to the RPi compatible connector (see chapter 6.7 for details).

## 6.14 Board ID

The processor module can read the SBCs board ID code from the 2-Kbit serial EEPROM AT24MAC402. The EEPROM is connected to the I²C interface I2C1 of the STM32MP157.

- The 2-Kbit-EEPROM is available via the 7bit device address 0x50.
- The extended memory block with a 128bit serial number is available via the 7bit device address 0x58.
- The write-protect registers of the device are accessed via the 7bit device address 0x30.

## 6.15 User-LEDs

The emSBC-Argon is equipped with a bicolor LED D3 (red and green). The LEDs are controlled by GPIOs PF12 and PE7.

The signals to control the LEDs are low-active, i.e. the LEDs are turned on while the GPIO is driven low.

| Pin | Signal | CPU Pin Name | Module Pin | SBC function |
|---|---|---|---|---|
| - | GPIO_01 | PF12 | 15 | Red LED |
| - | GPIO_00 | PE7 | 16 | Green LED |

Please watch that the red LED at GPIO PF12 is connected in parallel to the ADC1 input. Therefore, the ADC input at connector J10, Pin 2 of the emSBC-Argon cannot be used.

## 6.16 GPIO-Connector

The emSTAMP-Argon provides a single-row pin-header J10 with 8 pins in 100mil pitch.

| Pin | Signal | CPU Pin Name | Module Pin |
|---|---|---|---|
| **1** | GND | | |
| **2** | GPIO_1 | PF12 | 15 |
| **3** | GPIO_0 | PE7 | 16 |
| **4** | SAI2_MCLK_A | PE0 | 48 |
| **5** | DAC1_OUT1 | PA4 | 39 |
| **6** | DAC1_OUT2 | PA5 | 38 |
| **7** | TIM1_CH1 | PE9 | 11 |
| **8** | TIM1_CH1N | PE8 | 12 |

## 6.17 Power Supply

The emSBC-Argon board is supplied by the DC-power jack J14 (Type: KLDX-SMT-0202-AP from KYCON). The board has to be supplied with a voltage between 7VDC and 24VDC. The input supply voltage is protected from reverse polarity and overvoltage.

A 5.0 VDC switching regulator with up to 2.5 A output current is populated on the SBC-board to provide the necessary 5.0 VDC input voltage for the emSTAMP-module. The maximum power consumption of the SBC is limited by the switching regulator to 12.5W.

# 7 Technical Characteristics

## 7.1 emSTAMP-Argon (CPU-Modul)

### 7.1.1 Electrical Specifications

| | |
|---|---|
| **Nominal supply voltage** | + 5.0V ± 5% |
| **max. current consumption** | 0.30A @ 5.0V |

### 7.1.2 Environmental Specifications

| | |
|---|---|
| **operating temperature** | -40°C ... +85°C |
| **storage temperature** | -40°C ... +125°C |
| **relative humidity** | 0 ... 95 %, non-condensing |

### 7.1.3 Mechanical Specifications

| | |
|---|---|
| **weight** | 7g |
| **dimensions** | 32.0 mm x 32.0 mm x 3.2 mm |

## 7.2 emSBC-Argon (Single Board Computer)

### 7.2.1 Electrical Specifications

| | |
|---|---|
| **supply voltage** | +7V to +24V |
| **max. current consumption** | 0.20A @ 12.0V |

### 7.2.2 Environmental Specifications

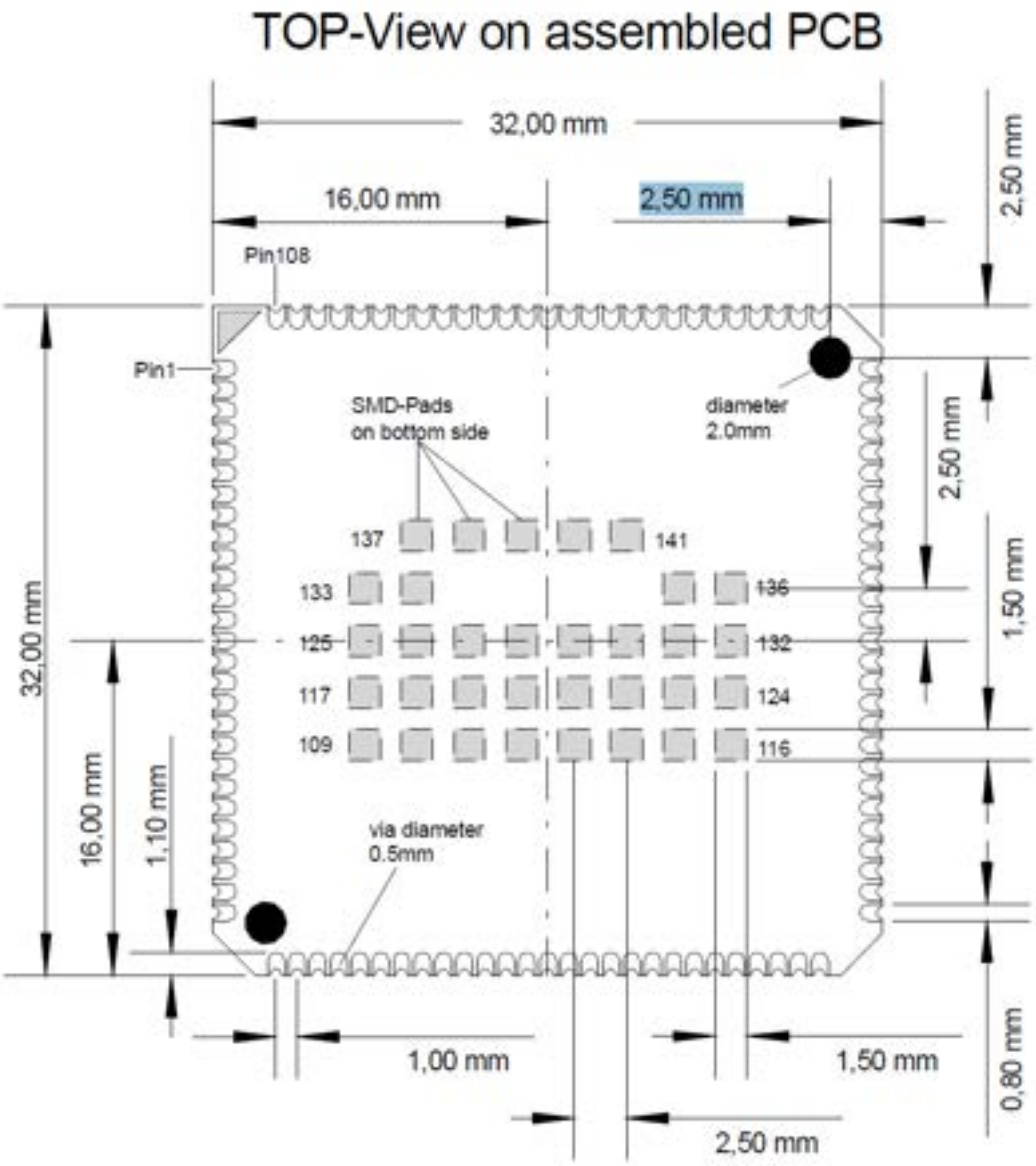
| | |
|---|---|
| **operating temperature** | -25°C ... +85°C |
| **storage temperature** | -25°C ... +85°C |
| **relative humidity** | 0 ... 95 %, non-condensing |

### 7.2.3 Mechanical Specifications

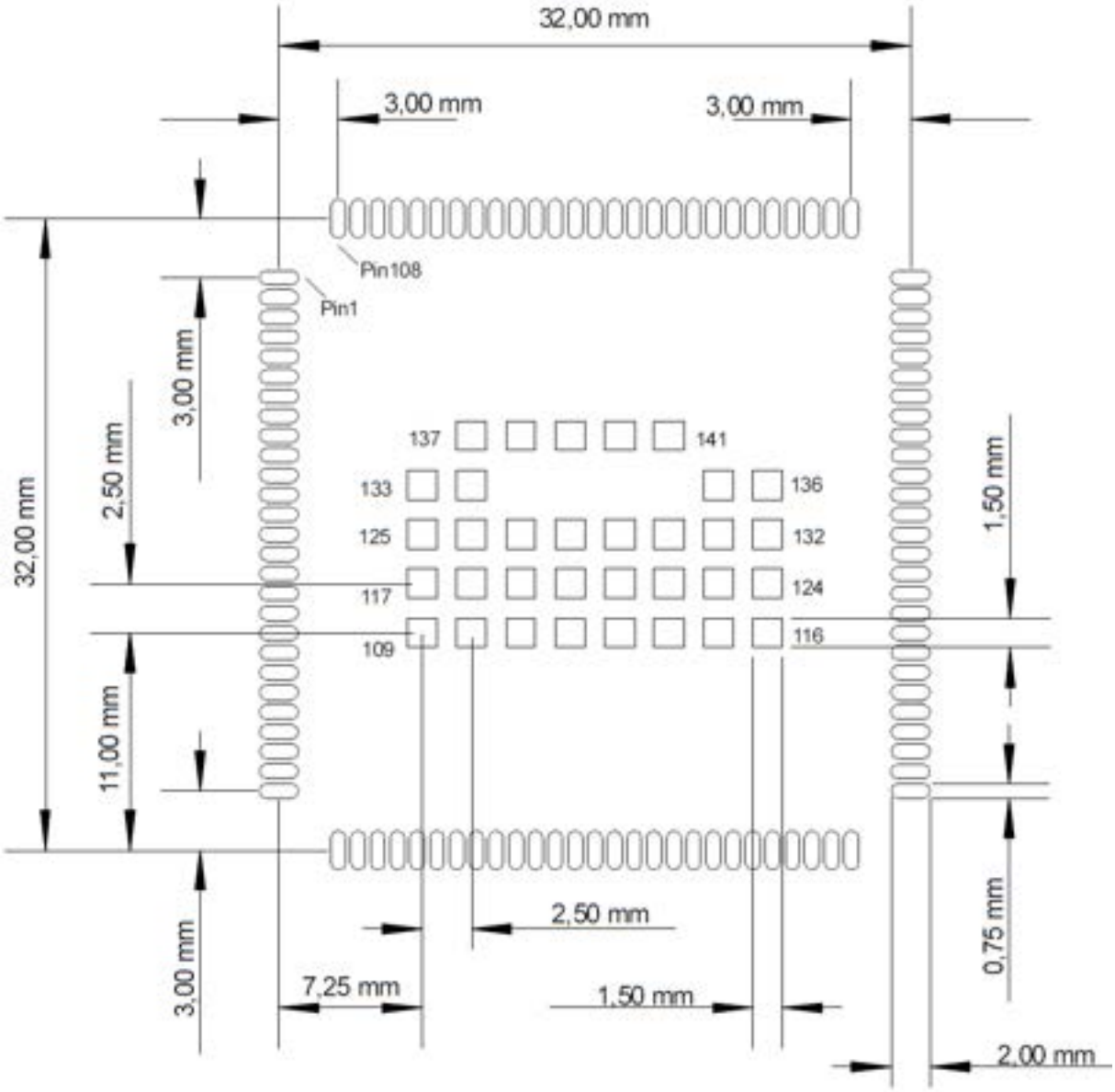
| | |
|---|---|
| **weight** | 55 g |
| **dimensions** | 104.5 mm x 77.5 mm x 16 mm |

## 7.3 Dimensional Drawings

### 7.3.1 emSTAMP-Argon (CPU module)



### 7.3.2 Recommended footprint (CPU module)




Layout Notes:

1. Try to avoid long routes on top layer beneath module. Via fanout beneath module is acceptable.
2. If the center pads 109 to 141 are not used, keep this area on the top layer free from routes and vias.

### 7.3.3 Assembly drawing emSBC-Argon (SBC)